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10/789,117	02/27/2004	Louis B. Hobson	200314976-1	7606

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EXAMINER	
LO, SUZANNE	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/789,117	HOBSON, LOUIS B.	
	Examiner	Art Unit	
	Suzanne Lo	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Additionally, MPEP 2114 states:

APPARATUS CLAIMS MUST BE STRUCTURALLY DISTINGUISHABLE FROM THE PRIOR ART

>While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

2. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claims 1 and 12-13, the phrase "capable of being" renders the claim indefinite because it is unclear whether the limitation is given patentable weight. Claims 2-11 by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the

invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-4, 6-21, and 23-24 are rejected** under 35 U.S.C. 102(e) as being clearly anticipated by **Bhatia et al. (U.S. Patent No. 6,535,798 B1).**

As per claim 1, Bhatia is directed to a system for simulating a processor performance state, comprising: a data structure stored in a memory, the data structure being configured to store an address of an ACPI throttling register, and a set of bit patterns that may be written to the ACPI throttling register **(column 12, lines 38-57)**, and a logic configured to receive a request to establish a desired processor performance state in a processor, to select a bit pattern from the set of bit patterns to be written to the ACPI throttling register, and to cause the processor to be throttled in a manner that simulates the desired processor performance state by writing the selected bit pattern to the ACPI throttling register **(column 9, lines 12-26)**.

As per claim 2, Bhatia is directed to the system of claim 1, where the data structure is further configured to store an address of an ACPI status register from which a value related to a throttling status established by the ACPI throttling register can be read **(column 12, lines 40-43)**.

As per claim 3, Bhatia is directed to the system of claim 1, where the memory is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions **(column 7, lines 57-65)**.

As per claim 4, Bhatia is directed to the system of claim 1, where the data structure comprises an ACPI table stored in a memory that is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions **(column 7, lines 57-65)**.

As per claim 6, Bhatia is directed to the system of claim 1, where the set of bit patterns facilitates simulating two processor performance states that correspond to a higher performance state and a lower performance state **(column 5, lines 22-25)**.

As per claim 7, Bhatia is directed to the system of claim 1, where the set of bit patterns facilitates simulating four processor performance states **(column 8, lines 55-61)**.

As per claim 8, Bhatia is directed to the system of claim 1, where the set of bit patterns facilitates simulating two or more processor performance states **(column 9, lines 46-48)**.

As per claim 9, Bhatia is directed to the system of claim 8, where the two or more processor performance states include eight processor performance states simulated by throttling the processor 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, and 87.5% of the time **(column 8, lines 55-61)**.

As per claim 10, Bhatia is directed to the system of claim 1, where the ACPI throttling register is configured to cause the processor to be throttled by asserting a signal on a line connected to the processor **(column 4, lines 8-24)**.

As per claim 11, Bhatia is directed to the system of claim 10, where the line comprises the STOPCLK# line **(column 13, lines 63-67)**.

As per claim 12, Bhatia is directed to a computer configured with a system for simulating a processor performance state, the system comprising: a data structure stored in a memory, the data structure being configured to store an address of an ACPI throttling register and a set of bit patterns that may be written to the ACPI throttling register **(column 12, lines 38-57)**, and a logic configured to receive a request to establish a desired processor performance state in a processor, to select a bit pattern from the set of bit patterns to be written to the ACPI throttling register, and to cause the processor to be throttled in a manner that simulates the desired processor performance state by writing the selected bit pattern to the ACPI throttling register **(column 9, lines 12-26)**.

As per claim 13, Bhatia is directed to a printer configured with a system for simulating a processor performance state, the system comprising: a data structure stored in a memory, the data structure being configured to store an address of an ACPI throttling register and a set of bit patterns that may be written to the ACPI throttling register **(column 12, lines 38-57)**, and a logic configured to receive

a request to establish a desired processor performance state in a processor, to select a bit pattern from the set of bit patterns to be written to the ACPI throttling register, and to cause the processor to be throttled in a manner that simulates the desired processor performance state by writing the selected bit pattern to the ACPI throttling register **(column 9, lines 12-26)**.

As per claim 14, Bhatia is directed to a method for simulating a processor performance state, comprising: receiving a request to establish a processor performance state in a processor **(column 12, lines 38-57)**; accessing a data structure to acquire a bit pattern to write to an ACPI throttling register and an address for the ACPI throttling register **(column 12, lines 38-57)**; and simulating a processor performance state by causing the processor to be throttled in response to writing the bit pattern to the ACPI throttling register **(column 9, lines 12-26)**.

As per claim 15, Bhatia is directed to the method of claim 14, including establishing the data structure as an ACPI table in a Basic Input Output System (BIOS) operably connectable to the processor **(column 7, lines 57-65)**.

As per claim 16, Bhatia is directed to the method of claim 15, where establishing the data structure includes writing a set of bit patterns to the ACPI table and writing the address of the ACPI throttling register to the ACPI table **(column 12, lines 40-43)**.

As per claim 17, Bhatia is directed to the method of claim 14, where the processor performance state corresponds to one of a higher performance state and a lower performance state **(column 5, lines 22-25)**.

As per claim 18, Bhatia is directed to the method of claim 14, where the processor performance state corresponds to one of two or more user defined processor performance states **(column 9, lines 46-48)**.

As per claim 19, Bhatia is directed to the method of claim 14, where the processor performance state corresponds to one of eight processor performance states including a state where the processor is

throttled one of 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, and 87.5% of the time **(column 8, lines 55-61)**.

As per claim 20, Bhatia is directed to the method of claim 14, where writing the bit pattern to the ACPI throttling register causes a signal to be asserted on a STOPCLK# line into the processor **(column 4, lines 8-24 and column 13, lines 63-67)**.

As per claim 21, Bhatia is directed to the method of claim 14, including: acquiring an address of an ACPI status register configured to report a value related to a throttling status of the processor **(column 12, lines 40-43)**; reading the value from the ACPI status register **(column 12, lines 40-43)**; and selectively reporting a success or error condition based on the value **(column 13, lines 8-18)**.

As per claim 23, Bhatia is directed to a system, comprising: means for accessing ACPI data **(column 12, lines 38-57)**; means for receiving a request to drive a processor into a processor performance state **(column 12, lines 38-57)**; and means for controlling a clock signal to the processor by writing data retrieved from the ACPI data to an ACPI throttling register, where controlling the clock signal simulates the processor performance state **(column 9, lines 12-26)**.

As per claim 24, Bhatia is directed to a set of application programming interfaces embodied on a computer-readable medium for execution by a computer component in conjunction with simulating a processor performance state in a processor by controlling an ACPI throttling register, comprising: a first interface for communicating a bit pattern data **(column 12, lines 38-57)**; a second interface for communicating an ACPI throttling register address data; and a third interface for communicating a state data, where the state data is related to a simulated processor performance state generated by applying the bit pattern data to a register identified by the register address data **(column 9, lines 12-26)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 5 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bhatia (U.S. Patent No. 6,535,798 B1).**

As per claim 5, Bhatia is directed to the system of claim 1, but fails to specifically disclose where the data structure comprises an ACPI table stored in a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions. However, Bhatia does disclose a data structure comprising an ACPI table that is operable connected to a BIOS which is functionally equivalent to the above limitation **(column 7, lines 57-65)**.

As per claim 22, Bhatia is directed to a computer-readable medium storing processor executable instructions operable to perform a method for simulating a processor performance state in a processor, the method comprising: establishing an ACPI table in a Basic Input Output System (BIOS) operably connectable to the processor, where establishing the ACPI table includes writing a set of bit patterns to the ACPI table, and writing an address of an ACPI throttling register to the ACPI table **(column 12, lines**

38-57); receiving a request to establish a processor performance state in the processor, where the processor performance state corresponds to one of a higher frequency state and a lower frequency state **(column 12, lines 38-57)**; accessing the ACPI table to acquire a bit pattern to write to the ACPI throttling register and an address for the ACPI throttling register **(column 9, lines 12-26)**; and causing a processor to simulate a processor performance state by throttling the processor by writing the bit pattern to the ACPI throttling register **(column 9, lines 12-26)**.

Although Bhatia does not specifically disclose establishing an ACPI table in BIOS, it does disclose a data structure comprising an ACPI table that is operable connected to a BIOS which is functionally equivalent to the above limitation **(column 7, lines 57-65)**.

Response to Arguments

5. Applicant's arguments filed 11/01/06 have been fully considered but they are not persuasive.

6. The 35 U.S.C. 112, 2nd rejections of claims 1-13 are maintained as the amendment to the claims have not cured the previously stated deficiencies.

7. The objection to the drawings – Figures 1-8 – are maintained. Applicant has failed to demonstrate any features in the drawings that have not been taught by prior art. Furthermore, the majority of the drawings do not include any of the alleged new and distinct features claimed by the Applicant.

Response to 101 Arguments

8. The 35 U.S.C. 101 rejections of claims 1-24 are maintained. The position of the PTO is based on case law as clearly illustrated below. If it appears that the Patent Office's position has changed for example, the discrepancies between the Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility and the much older and indeed, possibly outdated PTO training materials

published in 1996, it is due to the fact that the PTO position is based on the most recent case law. Furthermore, the language used in clarifying the 101 rejections in the previous Office Action is irrelevant. Regardless of the Applicant's dismissal of the "feelings" of the Office, the "feelings" or the Position of the Office is and has always been based on statues and case law.

As the Applicant appears to misconstrue the eligibility of the submitted claims in terms of statutory subject matter, a thorough analysis of the claims in terms of patent eligibility is disclosed below.

Claim 1

The system of claim 1 only states software – a system with a data structure and logic. As such, claim 1 is directed to functional descriptive material without an embodiment on medium or a machine that is structurally or functionally related. As the functional descriptive material is not combined with a medium, it is software, *per se* which is non-statutory. See Warmerdam, 33 R.3d at 1361, 31 USPQ2d at 1760.

Claims 2-11 do not cure this deficiency, the dependent claims are still directed to functional descriptive material without an embodiment on medium or a machine, or software, *per se*.

Claims 12, 13, 23 are similarly deficient with a computer or printer configured with a system with functional descriptive material without embodiment on medium or a machine that is structurally or functionally related.

Claim 14

The method of claim 14 is so broadly claimed that it can be directed to software only. In order to be patent eligible, the method must either provide a physical transformation or provide a practical application that produces a useful, tangible, and concrete result. See AT&T, 172 F.3d at 1358-59, 50 USPQ2d at 1452. As the method does not produce a physical transformation, must provide a useful,

tangible and concrete result. The changes of the values of the ACPI register only modifies values within software with no real-world result. As the aforementioned method does not permit the function of the descriptive material to be realized, the method provides no substantial practical application without a tangible result, the method of claim 14 is not patent eligible. See Benson, 409 U.S. at 71-72, 175 USPQ at 676-77 and MPEP 2106.01.

Claims 15-21 do not cure this deficiency, the dependent claims are still directed to a process without producing a physical transformation or producing a useful, tangible, and concrete result.

Claim 22

As claim 22 is directed to computer-readable medium storing processor executable instructions operable to perform a method with steps similar to claim 14, it must also provide either provide a physical transformation or provide a practical application that produces a useful, tangible, and concrete result. However, the method does not produce a physical transformation but only modifies values within software with no real-world result. Again, the function of the descriptive material is not realized and the claims provides no substantial practical application without a tangible result. See Benson, 409 U.S. at 71-72, 175 USPQ at 676-77 and MPEP 2106.01.

Claim 24

Claim 24 is treated similarly to claim 22 as it is directed to a set of application programming interfaces, or software, embodied on a computer-readable medium. The interfaces are not functional, they do not produce a physical transformation nor do they provide a practical application that produces a useful, tangible and concrete result. In fact, claim 24 appears to be directed only towards nonfunctional descriptive material, which is non statutory. See Diehr, 450 U.S. at 185-86, 209 USPQ at 8.

Rejections of claims 22 and 24 due to the non statutory subject matter of carrier waves

Upon examination of claims 22 and 24 and case law, carrier waves or "manufacture transient phenomenon", as Applicant defines them, are non statutory as they do not fall into any of the statutory categories.

The carrier waves, or manufactured temporary events, are not a process; they are not a series of steps.

The carrier waves, or manufactured temporary events, are not a machine; they have no physical structure. "The term machine includes every mechanical device or combination of mechanical device or combination of mechanical powers and devices to perform some function and produce a certain effect or result." Corning v. Burden, 56 U.S. (15 How.) 252,267 (1854).

The carrier waves, or manufactured temporary events, are not composition of matter; it is not matter, but a form of energy. A "composition of matter" "covers all compositions of two or more substances and includes all composite articles, whether they be results of chemical union, or of mechanical mixture, or whether they be gases, fluids, powders or solids." Shell Development Co. v. Watson, 149 F. Supp. 279, 280, 113 USPQ 265, 266 (D.D.C. 1957), aff'd, 252 F.2d 861, 116 USPQ 428 (D.C. Cir. 1958).

The carrier waves, or manufactured temporary events, are not a product of manufacture; as read by the Supreme Court, the definition of product of manufacture requires physical substance which the carrier waves do not have. See Diamond v. Chakrabarty, 447 U.S. 303, 308, 206 USPQ 193, 196-97 (1980) (quoting American Fruit Growers, Inc. v. Brogdex Co., 283 U.S. 1, 11, 8 USPQ 131, 133 (1931), which, in turn, quotes the Century Dictionary).

As signals do not fall under any statutory category, the 35 U.S.C. 101 rejections of claims 22 and 24 are maintained. Additionally, the signals claimed as a "manufactured transient phenomenon" may be

analogous to a floppy disk and other statutory products of manufacture but they *are not* a product of manufacture as defined by case law.

In order to overcome the 101 rejections of claims 22 and 24, Applicant's definition of a "manufactured transient phenomenon" must comply with court established definitions of a statutory category (machine or product of manufacture). Applicant has failed to show why the claimed signals fall under any statutory category and has failed to provide evidence to support Applicant's allegation of "manufactured transient phenomenon" as statutory.

Response to Prior Art Arguments

9. Claims 15 and 22

In response to Applicant's argument that Bhatia does not disclose "establishing an ACPI table in a BIOS" the Applicant is directed to **column 7, lines 57-64** "the thermal management routine may be implemented in BIOS" and **column 3, lines 15-19** as the thermal management routine includes the data structure therefore disclosing implementing an ACPI table in a BIOS.

The Examiner thanks Applicant for pointing out the inconsistency of the rejections of claims 15 and 22. As stated above Bhatia does indeed teach implementing or "establishing" the data structure in BIOS.

Claim 1

In response to Applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which the Applicant relies (i.e., simulation without true processor performance state change) are not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, the enablement of the invention is specified by optional language –

"simulation *may* be transparent"

"processor *may* not include internal machine"

"processor *may* produce a simulated processor performance"

and even in light of the specification of the instant application, and the aforementioned limitations are not required by the enablement.

In response to the Applicant's argument that Bhatia does not teach storing bit patterns but rather store values for controlling throttling. As well known in the art, the bit patterns for controlling throttling is part of the ACPI specification **(column 1, lines 7-38)**. In storing control values for throttling within the ACPI environment **(column 3, lines 15-19)**, Bhatia clearly anticipates storing, selecting and writing bit patterns.

Additionally, closer examination of cited passage Bhatia, **column 9, lines 12-26** reveal that selecting a bit pattern is clearly anticipated.

Text	Claim Interpretation	Teaches Selecting Bit Pattern?
A clock duty cycle setting representing the current performance level Pn may be written by a thermal management module....to a control register....to define the percentage of maximum performance desired of the processor 12.	Bit pattern (clock duty cycle setting) is written, definition of a specific desired performance percentage produced by selection of a particular bit pattern	Yes

The control register is accessible by hardware control logic to control activation and deactivation of the processor's clock control input.	Control activation and deactivation determined by bit pattern, the differentiation of activation and deactivation requires bit pattern selection	Yes
The number of register bits dedicated to store the clock duty cycle settings determines the number of different duty cycles settings that may be made by the hardware control logic.	Change between different duty cycles are regulated by different bit patterns, clock duty cycle settings set by bit pattern selection	Yes

Subsequently, dependent claims 2-12 are still rejected as are claims 12-21 for the same reasons.

Claim 5

As noted above in regards to claims 15 and 22, the Applicant is directed to **column 7, lines 57-64** "the thermal management routine may be implemented in BIOS" and **column 3, lines 15-19** as the thermal management routine includes the data structure therefore disclosing implementing an ACPI table in a BIOS.

Claim 6, 8-9

As noted above in regards to claim 1, the features upon which the Applicant relies (i.e., simulation without true processor performance state change) are not recited in the rejected claim.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, the enablement of the invention is specified by optional language –

"simulation *may* be transparent"

"processor *may* not include internal machine"

"processor *may* produce a simulated processor performance"

and even in light of the specification of the instant application, and the aforementioned limitations are not required by the enablement.

Claims 7, 11

In response to Applicant's argument that Bhatia does not disclose wherein the processor does not have a variable voltage supply (claim 7) and variable frequency clock (claim 11), it is well known in the art as part of the ACPI Standards **(column 1, lines 7-38)** that the voltage source and clocking source are not variable, but rather the variation occurs from the throttling only through the actions of the processor are the received signals within the processor varied; the sources themselves are not variable.

Claims 16, 21

In response to Applicant's argument that Bhatia does not disclose reading and writing the ACPI address, in working with the control register and definition of different performance states, reading and writing of the address of the control register is inherent within the ACPI Specification in order to allow the access to and modification of said control register.

Claim 23

As noted above in regards to claim 1, the features upon which the Applicant relies (i.e., simulation without true processor performance state change) are not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, the enablement of the invention is specified by optional language –

"simulation *may* be transparent"

"processor *may* not include internal machine"

"processor *may* produce a simulated processor performance"

and even in light of the specification of the instant application, and the aforementioned limitations are not required by the enablement.

Claim 24

Applicant's argument that Bhatia only discloses interfaces residing in a computing system rather than on a computer readable medium for execution by a computer component is mere allegation without providing evidence. The interface for communicating the ACPI throttling register address data is inherent within the ACPI interface which includes the interface for communicating state data. Furthermore, as known to any ordinary person skilled in the art, the state data is data needed for controlling states; in writing control data, the state data is read from the status register, the reading of the state data and writing of the control register is the communication of the state data.

Conclusion

10. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references include:

1. U.S. Patent No. 7,082,542 B2 issued to Cooper on 07/25/06.

2. U.S. Patent No. 6,122,748 issued to Hobson on 09/19/00.

12. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suzanne Lo
Patent Examiner
Art Unit 2128

SL
01/19/07

KAMINI SHAH
SUPERVISORY PATENT EXAMINER